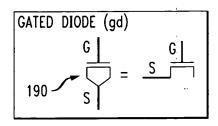


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FIG. 1A



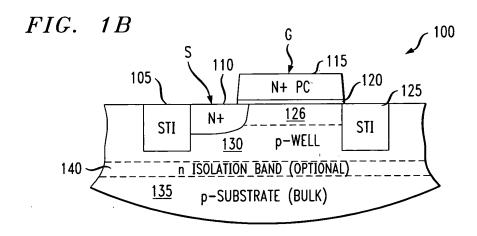


FIG. 1C

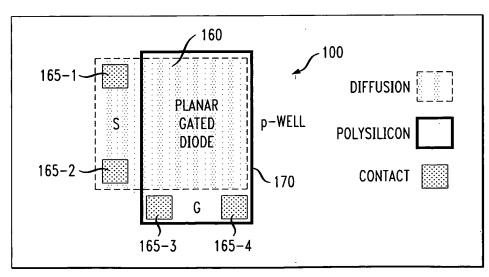
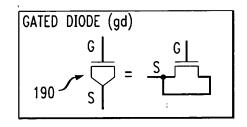


FIG. 2A



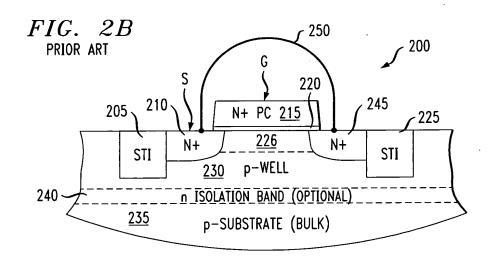


FIG. 2C

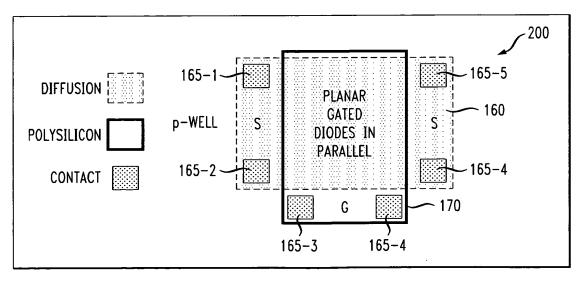


FIG. 3A

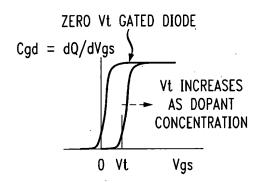


FIG. 3B

GATED DIODE CAPACITANCE vs GATE-TO-SOURCE VOLTAGE (Vgs) EACH CURVE REPRESENTS A DIFFERENT GATED DIODE GATE SIZE.

THRESHOLD VOLTAGE = 0.2 V

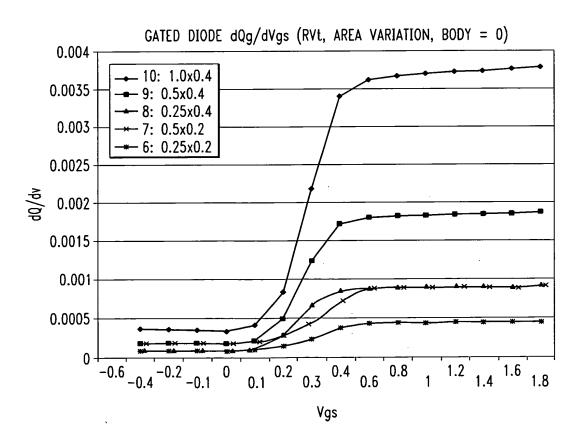


FIG. 4A

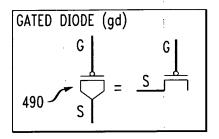


FIG. 4B

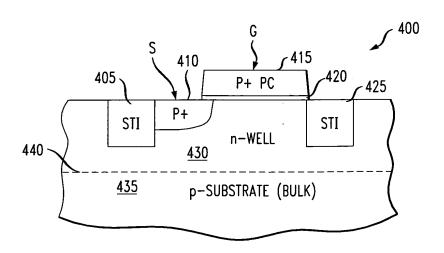


FIG. 5A

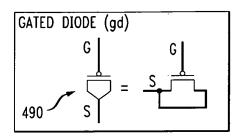


FIG.~5B PRIOR ART:

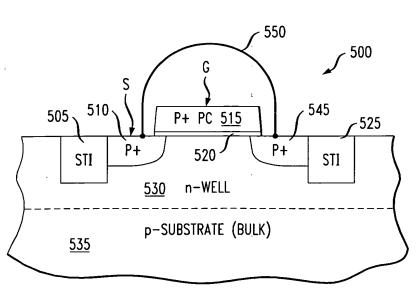


FIG. 6

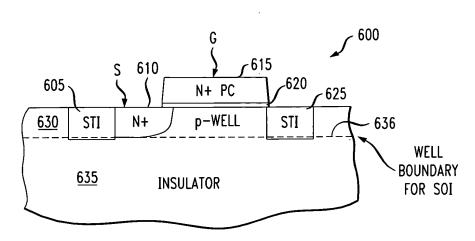
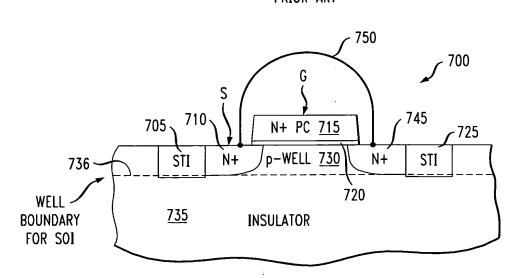
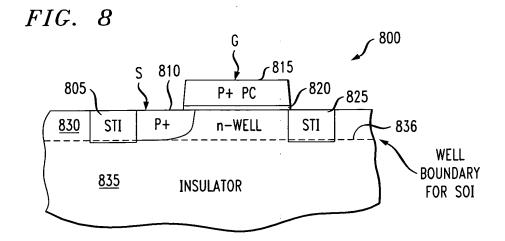


FIG. 7
PRIOR ART



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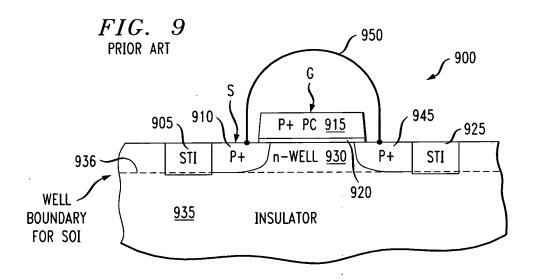


FIG. 10

LINEAR CAPACITOR

GAIN = dVout/dVin = 1

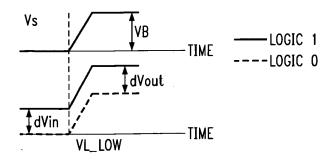
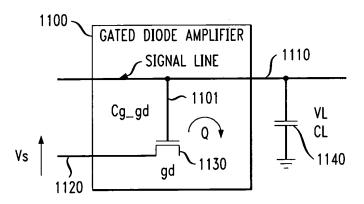
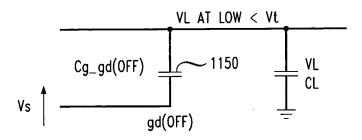


FIG. 11A



 $FIG.\ 1\,1B$ gated diode amplifier representative circuit



 $FIG.\ 11C$

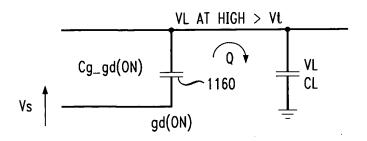


FIG. 12A

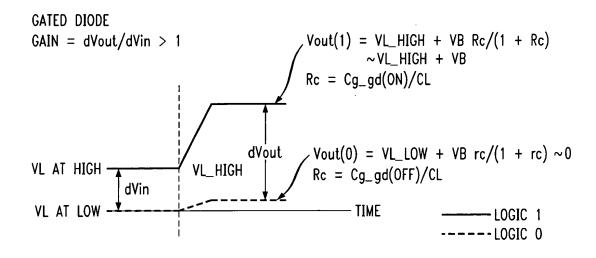


FIG. 12B

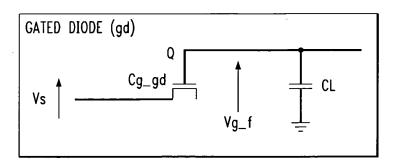


FIG. 12C

$Rc = Cg_gd/CL$ $GAIN = Vg_f/Vg_i$									
GAIN = 1 + Rc - (Vt_gd/Vg_i) Rc ~ 1 + Rc GAIN = $(1 + Vs/Vg_i)$ Rc/ $(1 + Rc)$	ld/Vg_i) Rc/(1 +	Rc ~ 1 Rc)	+ Rc	COMP	LETE CH TRAINED	ARGE TRA CHARGE	insfer (i Transfei	COMPLETE CHARGE TRANSFER (FOR SMALL Rc) CONSTRAINED CHARGE TRANSFER (LARGE Rc)	
$Vg_{-}i = 0.4 \text{ V}, Vt_{-}gd = 0$	0				EXEM	EXEMPLARY OPERATING POINT	ERATING	POINT	
Cg_gd/Cg_rg 1 + Rc Rc/(1 + Rc) (1+Vs/Vg_i)Rc/(1+Rc) (1+Vs/Vg_i)Rc/(1+Rc) GAIN CHARGE TRANSFER	0.01 1.01 0.01 0.035 0.04 1.01	0.1 1.1 0.09 0.32 0.36 1.1 COMPLETE	1 2 0.5 1.75 2.00 2	2 3 0.67 2.35 2.68 2.68	5 6 0.83 2.91 3.32 3.32 CONST	10 11 3.19 3.64 3.64 RAINED	100 101 0.99 3.47 3.96 3.96	Vs/Vg = 2.5 Vs/Vg = 3 Vs/Vg = 3	



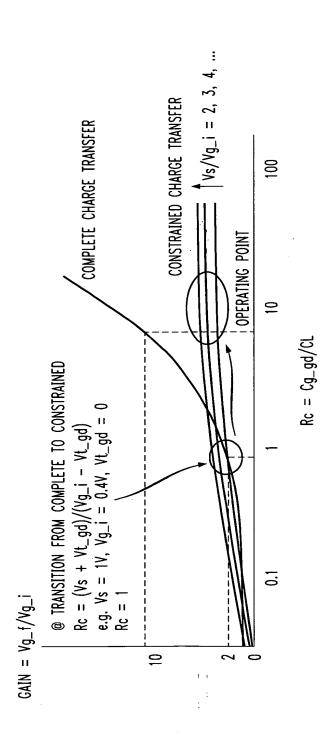


FIG. 13

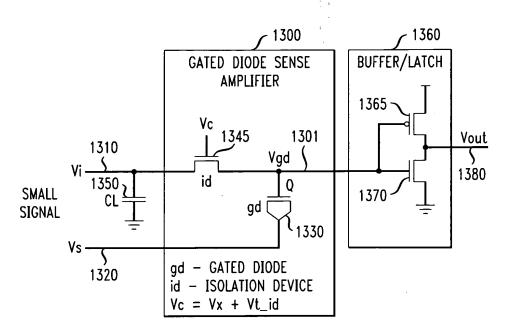


FIG. 14

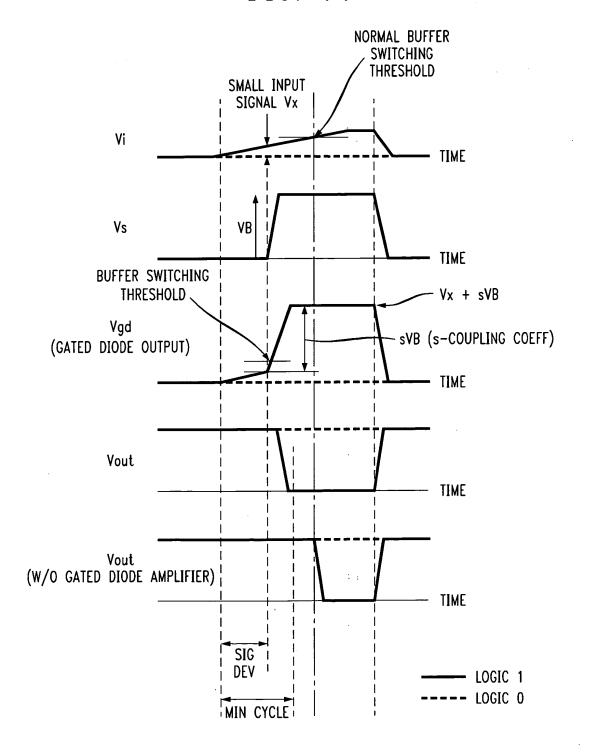


FIG. 15

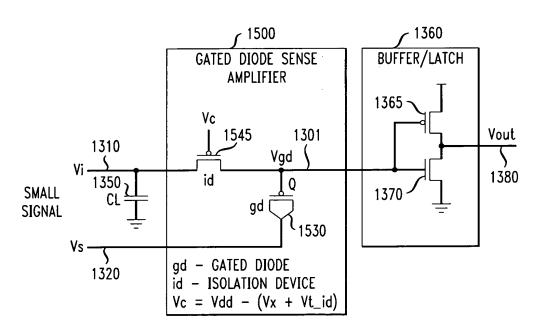
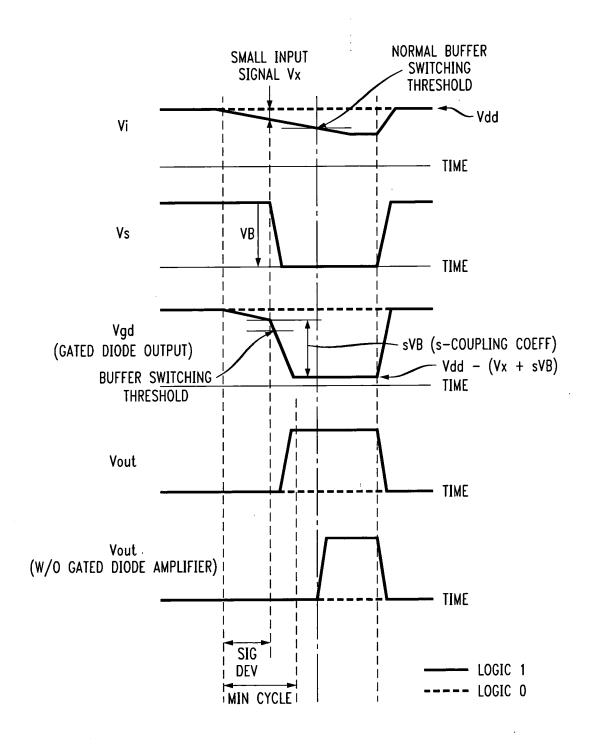


FIG. 16



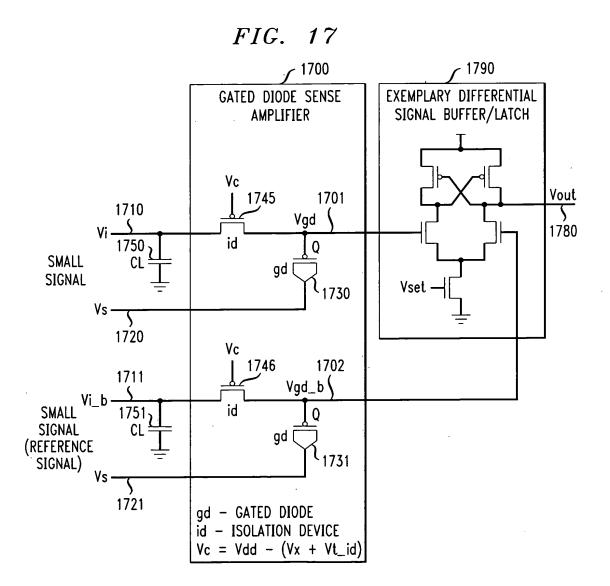
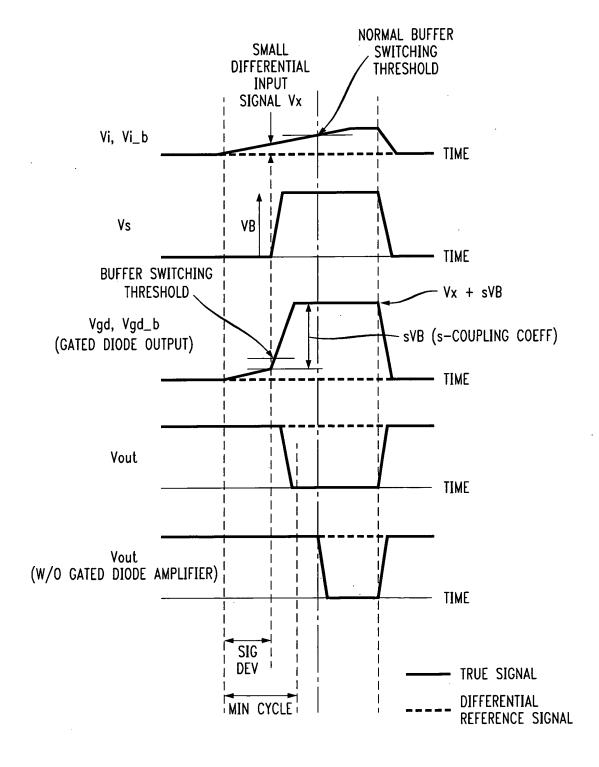


FIG. 18



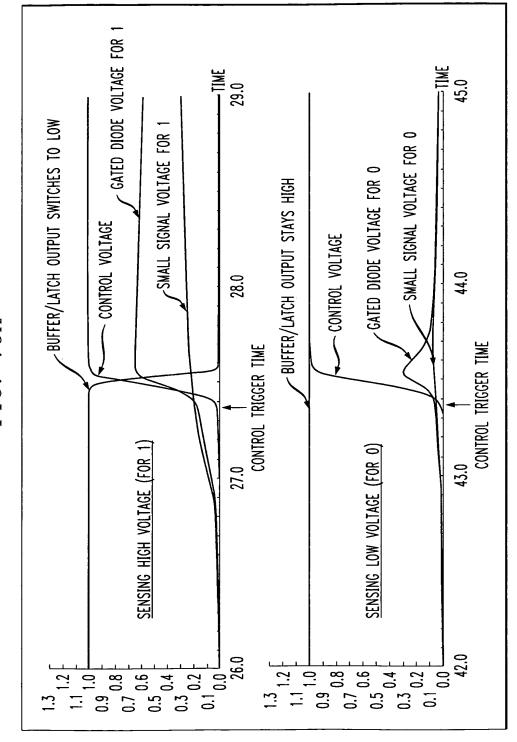


FIG. 19A

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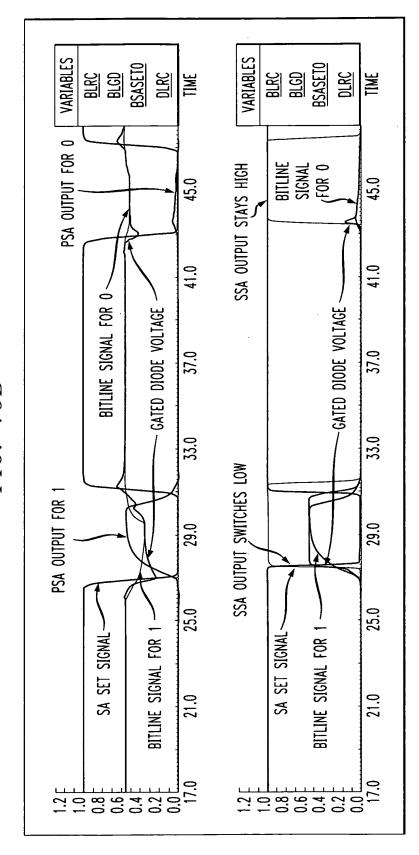


FIG. 19B

FIG. 20A

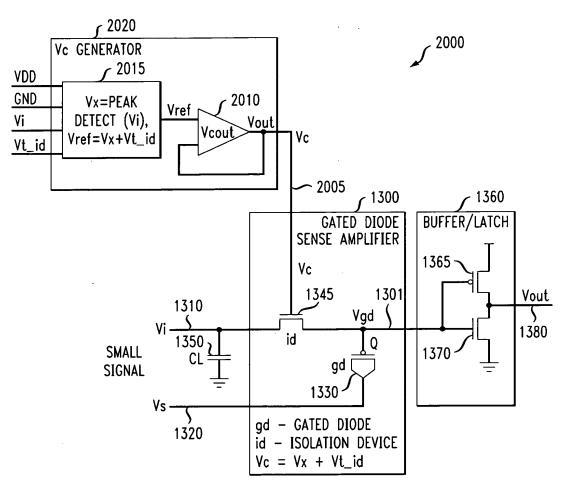


FIG. 20B

